CLMPTO
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CLAIMS 1-15. (CANCELLED)

16. A method of reading n ($n \geqq 2$) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., and Xn), comprising the steps of:

converting a logical address into a physical address included in the physical address space;

judging whether a logical address space including the logical address matches the physical address space;

specifying the most significant bit X1 by applying a predetermined reference voltage to a gate of the transistor to determine whether a current flows between a source and a drain of the transistor when the logical address space matches the physical address space; and

outputting the specified bit from one of the cells corresponding to the physical address.

17. The method according to claim 16 further comprises the step of specifying the bits (X1, X2, ..., Xn) by applying maximum n number of different reference voltages to the gate of the transistor at a specific voltage applying order until a current flows between the source and the drain when judged that the logical address space does not match the physical address space.

CLAIMS 18-21 (CANCELLED)

22. A computer readable medium storing program code for causing a computer to read n ($n \geqq 2$) number of bits (X1, X2, ..., Xn) from a plurality of multilevel memory cells arranged so as to correspond to a physical address space, each cell having at least one transistor, each cell storing 2^n levels of data each expressed by the bits (X1, X2, ..., Xn), comprising:

first program code means for converting a logical address into a physical address included in the physical address space;

second program code means for judging whether a logical address space including the logical address matches the physical address space;

third program code means for specifying the most significant bit X1 by applying a reference voltage to a gate of the transistor when the logical address space matches the physical address space to determine whether a current flows between a source and a drain of the transistor; and

fourth program code means for outputting the specified bit from one of the cells corresponding to the physical address.

23. The computer readable medium according to claim 22 further comprising the program code means for specifying the bits (X1, X2, ..., Xn) by applying maximum n number of different reference voltages to the gate of the transistor at a specific voltage applying order until a current flows between the source and the drain when judged that the logical address space does not match the physical address space.

CLAIMS 24-68. (CANCELLED)